Compute Express Link (CXL) is an open industry interconnect standard for providing high bandwidth and low latency. It adds connectivity between host processors, accelerators, memory devices, and network interface cards (NICs). CXL also enables memory expansion and acceleration across high-performance computational workloads for AI, ML, HPC, and communications segments. CXL uses PCIe Gen 5.0 PHY based high-speed serial link to communicate between the latest generation of CPU processors.

SMART develops CXL Type 3 (CXL.mem) memory products to address the industry’s need for more memory per processor core. The CXL interconnect specification allows for a significant expansion of memory form factor options leveraged from SSDs. SMART’s introductory CXL Memory Modules known as XMM are offered in the E3.S form factor.

**Key Features**
- CXL-2.0 compatible with PCIe-Gen5 speeds running at 32GT/s
- Available in 64GB DDR5 memory capacity with expansion up to 256GB in future
- Supports Reliability, Availability and Serviceability (RAS) features added in CXL-2.0
- Powered by only 12V supply from EDSFF compatible edge interface (SFF-TA-1009)
- Supports sideband interfaces for real-time debug, management and system update, enabling out-of-band management of the module
- Supports additional security features to protect data from side-channel attacks

**Why choose SMART Modular for CXL?**
- SMART is a contributing member of the CXL consortium, closely collaborating with CPU and silicon suppliers to test for compatibility and feature completeness.
- SMART has PCB design and assembly to develop high speed memory and storage modules in variety of form-factors like DIMMs, E1.S, E3.S and PCIe add-in cards.
- SMART’s global manufacturing footprint and strong relationships with components suppliers minimizes disruption even in stringent supply-chain conditions.
- Customers can leverage SMART’s test and validation service for pre-screening memory modules for reliability and quality.
- SMART’s engagement in other emerging technologies like Gen-Z, OpenCAPI and persistent memory solutions such as NVDIMM-N.
Applications

- Disaggregated pool of shared memory for HPC applications accessible over CXL fabric
- Secure memory for managing trusted keys and in-memory database
- OLTP Log Cache Acceleration
- In-line compression, encryption or vector atomic operations, transparent to CPU while using normal memory load/store semantics
- Targeted for 2U servers to enables memory expansion with up to 16 E3.S modules in single 2U server achieving better throughput than direct attached DDR5 DIMMs.

Ordering Information

<table>
<thead>
<tr>
<th>CXL Memory Module (XMM)</th>
<th>SMART Part Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>STXAB64GK4Q18SM</td>
<td>128GB FPGA based CXL-2.0 E3.S Memory module with dual ranks/channel x64 + ECC DDR4</td>
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<td></td>
<td></td>
<td>With user customizable FPGA logic for adding in-band acceleration functions like compression and encryption</td>
</tr>
<tr>
<td></td>
<td>STXAB64G4Q36SA</td>
<td>64GB FPGA based CXL-2.0 E3.S Memory module with dual ranks/channel x64 + ECC DDR4</td>
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<tr>
<td></td>
<td></td>
<td>User customizable FPGA logic for adding in-band acceleration functions like compression and encryption</td>
</tr>
<tr>
<td></td>
<td>STXAB64G4Q4OSB</td>
<td>64GB ASIC based CXL-2.0 E3.S Memory module with dual ranks/channel x64 + ECC DDR5</td>
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<tr>
<td></td>
<td></td>
<td>Suitable for low-latency memory expansion</td>
</tr>
</tbody>
</table>

Contact: Arthur Sainio at Arthur.Sainio@smartm.com for any sales and sampling queries.